Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A data processing system for qualifying events when an interrupt occurs, comprising:

an interrupt unit control mechanism for indicating an interrupt of a selected type;

an interrupt unit, responsive to an interrupt, for determining if the interrupt is an interrupt of the selected type;

a performance monitoring unit; and

one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count the occurrence of events during processing of [[an]] the interrupt responsive to a determination by the interrupt unit that the interrupt is an interrupt of [[a]] the selected type.

2. (Original) The system of claim 1, wherein the one or more hardware counters count the occurrence of events during a state of the interrupt of the selected type.

3. (Previously presented) The system of claim 2, wherein states of the interrupt include interrupt on, interrupt taken and interrupt acknowledged.

4. (Previously presented) The system of claim 1, wherein multiple types of events are counted during the processing of the interrupt.

5. (Previously presented) The system of claim 1, wherein the one or more hardware counters count the occurrence of events according to the type of interrupt during which the events occur.

6. (Original) The system of claim 1, wherein the events include clock cycles and cache misses.

7. (Previously presented) The system of claim 1, wherein a second interrupt interrupts the interrupt of the selected type, and wherein the hardware counters count events separately that occur during the processing of the interrupt of the selected type and during processing of the second interrupt.

8. (Previously presented) A method of executing instructions on an information processing system, comprising the steps of:

receiving a signal at a microprocessor of the system for invoking an interrupt, wherein the interrupt includes a plurality of states; and

counting at least one event for a selected state of the plurality of states during processing of the interrupt.

9. (Previously presented) The method of claim 8, wherein the step of counting includes counting at least one event for each of the plurality of states during the processing of the interrupt.

10. (Previously presented) The method of claim 8, wherein the plurality of states include interrupt on, interrupt taken and interrupt acknowledged.

11. (Original) The method of claim 8, wherein the at least one event includes clock cycles and cache misses.

12. (Previously presented) The method of claim 8, wherein the step of counting includes counting multiple types of events for the same state during the processing of the interrupt.

13. (Previously presented) The method of claim 8, wherein the step of counting is performed by one or more hardware counters during the processing of the interrupt.

14. (Previously presented) The method of claim 8, wherein the events are counted according to the type of interrupt during which the events occur.

15. (Previously presented) The method of claim 8, wherein the interrupt is interrupted by a second interrupt, and wherein hardware counters count events separately that occur during the processing of the interrupt and during processing of the second interrupt.

16. (Previously presented) A computer program product in a computer readable medium for processing instructions, the computer program product comprising:

first instructions for receiving a signal at a microprocessor of the system for invoking an interrupt, wherein the interrupt includes a plurality of states; and

second instructions for counting at least one event for a selected state of the plurality of states during processing of the interrupt.

17. (Previously presented) The computer program product of claim 16, wherein the plurality of states include interrupt on, interrupt taken and interrupt acknowledged.

18. (Previously presented) The computer program product of claim 16, wherein the at least one event includes clock cycles and cache misses.

19. (Previously presented) The computer program product of claim 16, wherein the second instructions for counting count multiple types of events for the same state during the processing of the interrupt.

20. (Previously presented) The computer program product of claim 16, wherein the step of counting is performed by one or more hardware counters during the processing of the interrupt.

21. (Previously presented) The computer program product of claim 16, wherein the events are counted according to the type of interrupt during which the events occur.

22. (Previously presented) The computer program product of claim 16, wherein the interrupt is interrupted by a second interrupt, and wherein hardware counters count events separately that occur during the processing of the interrupt and during processing of the second interrupt.

23. (New) A computer implemented method for qualifying events when an interrupt occurs, comprising:

indicating an interrupt of a selected type;

determining, responsive to an interrupt, if the interrupt is an interrupt of the selected type; and

responsive to determining that the interrupt is an interrupt of the selected type counting, by one or more hardware counters located within a performance monitoring unit, the occurrence of events during processing of the interrupt.